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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/761,539	01/16/2001	William J. Dally	2789.2010-000	5876

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LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER	
CHANG, RICHARD	
ART UNIT	PAPER NUMBER
2616	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/761,539	DALLY, WILLIAM J.	
	Examiner	Art Unit	
	Richard Chang	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,6,8-16,18,19 and 21-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *29* is/are allowed.

6)☒ Claim(s) *1-3,6,8-16,18,19 and 21* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on 01/10/2007, with respect to claims 1, 3, 6, 8-16, 18-19 and 21-28 have been fully considered but are moot in view of the new ground(s) of rejection. The subject matter of "the RAM comprises three buffers and the local frame counter include a modulo 3 counter field which selects one of the three buffers" in claims 1, 14 and 27, describes a broader structure without specifying its intended use of the three buffers in details. The finality of the last office action is withdrawn.

Claims 2, 4, 7, 17 and 20 had been canceled.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, 5-6, 8-10, 14-16, 18-23 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 6,778,529 ("Field et al.") in view of US patent No. 6,674,752 ("Colizzi et al.") and further in view of US patent No. 4,885,738 ("Bowers et al.").

Regarding claims 1, 14 and 27, Field et al. teach a method for a telecommunications synchronous switch node (time-slot interchanger) for interchanging the order of subframes of data (within an input data frame wherein each 125 microsecond frame period is divided into 256 subframes) comprising of

a global frame clock (a systems clock which is used to derive the 125 microsecond frame pulse for synchronization) (See Fig. 32, Col. 32, lines 12 - 26),

an interchange random access memory (switch memory 656) receiving the input data frame at an input (where the traffic may be directly received at the switch interface 650), out of alignment with the global frame clock (where the switch interface 650 provides the ingress TDM traffic storage independent of the global frame clock) (See Fig. 33, Col. 32, lines 27 - 62).

Field et al. teach substantially all the claimed invention but did not disclose expressly the particular application involving limitations of

"a write address generator which addresses the random access memory to write subframes, out of alignment with the global frame clock, in a received order", and

"a read address generator which addresses the random access memory to read subframes in interchanged order and aligned to the global frame clock".

Colizzi et al. teach a method and apparatus of switch matrix using independent read and write memory access for time slot interchange such that the memory is nonontiguoualy addressed and space mapped by the predecoder by storing subframes to the random access memory is controlled by the write address control memory (WCM) out of alignment with the global frame clock, in a received order and reading subframes

from the random access memory is controlled by the read address control memory (RCM) in interchanged order and aligned to the global frame clock (See Fig. 4, Col. 5, lines 38-54).

At the time the invention was made, therefore, it would have been obvious to one of ordinary skill in the art to which the invention pertains to combine Colizzi et al. with Field et al. to obtain a telecommunication synchronous time slot interchanging switch and to take advantage of providing a write address control memory (WCM) to store subframes to the random access memory, out of alignment with the global frame clock, in a received order and a read address Control Memory (RCM) to read subframes from the random access memory in interchanged order and aligned to the global frame clock.

The motivation to do so would have been to use independent read and write memory access for time slot interchange where storing subframes to the random access memory is controlled by the write address control memory out of alignment with the global frame clock, in a received order and reading subframes from the random access memory is controlled by the read address control memory in interchanged order and aligned to the global frame clock, as suggested by Colizzi et al. in Col. 5, lines 38-54.

Field et al. and Colizzi et al. teach substantially all the claimed invention but did not disclose expressly the particular application involving limitations of

"the RAM comprises three buffers and the local frame counter include a modulo 3 counter field which selects one of the three buffers".

Bowers et al. teach a similar method and apparatus of time-space switching network using memory access for time slot interchange and a common arrangement where the memory is arranged with three buffer structure to address time slot and frame alignment by using counter as buffer selector (See Fig. 1, Col. 2, line 57 to Col. 3, line 2).

At the time the invention was made, therefore, it would have been obvious to one of ordinary skill in the art to which the invention pertains to combine Browers et al. with Field et al. and Colizzi et al. to obtain a telecommunication synchronous time slot interchanging switch and to take advantage of a common arrangement with three buffer structure to address time slot and frame alignment by using counter as buffer selector to address memory access for time slot and frame interchange in three stages.

The motivation to do so would have been to arrange an three buffer structure to address time slot and frame alignment and use counter as buffer selector to address memory access for time slots and frames in three stages, as suggested by Bowers et al. in Col. 2, line 57 to Col. 3, line 2.

Regarding claims 3, 15-16, as discussed above, Colizzi et al. further teaches that a global frame counter count is used to access a random access memory (See Fig. 4, Col. 5, lines 38-54).

At the time the invention was made, therefore, it would have been obvious to one of ordinary skill in the art to which the invention pertains to combine Colizzi et al. with Field et al. to obtain a telecommunication synchronous time slot interchanging switch

and to take advantage of using a global frame counter count is used to access a random access memory.

The motivation to do so would have been to use a global frame counter count is used to access a random access memory, as suggested by Colizzi et al. in Col. 5, lines 38-54.

Regarding claims 5-6, 18-19, these claim have limitation that is similar to those of claim 1 and the official notice indicates that it is common to divide the temporarily storage memory into more then one buffer to support ping-pong type buffer swapping operations, and obviously the counter may support various buffer lengths, thus it is rejected with the same rationale applied against claim 1 above.

Regarding claims 8-9 and 21-22, these claim have limitation that is similar to those of claim 1 and the official notice indicates that the temporarily storage memory may be commonly a random access memory where noncontiguous addressing or the other way is merely a design choice, thus it is rejected with the same rationale applied against claim 1 above.

Regarding claims 10, 23, this claim has limitation that is similar to those of claim 9, and the official notice indicates that the total number of how many decoder in the predecoder is merely the designer's choice within a reasonable range, thus it is rejected with the same rationale applied against claim 9 above.

4. Claims 11-13, 24-26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 6,778,529 ("Field et al.") in view of US patent No.

6,674,752 ("Colizzi et al.") and US patent No. 4,885,738 ("Bowers et al.") and further in view of US patent No. 5,303,077 ("Buttle et al.").

Regarding claims 13, 26, 28, as discussed above, Colizzi et al. and Field et al. teach substantially all the claimed invention but did not disclose expressly the particular application involving limitations of

"at least one switch of at least one stage comprising a time-slot interchanger".

Buttle et al. teach an Optical switch and switching module, thus supports SONET STS-M frames, therefor wherein block 17 in dashed lines enclosing the time slot interchangers and the space switch 13 to indicate such a functional unit (at least one switch of at least one stage comprising a time-slot interchanger) (See Fig. 1, Col. 5, lines 30- 52).

At the time the invention was made, therefore, it would have been obvious to one of ordinary skill in the art to which the invention pertains to combine Buttle et al. with Colizzi et al. and Field et al. in order to obtain a time slot interchanger and to take advantage of the time slot interchangers and the space switch capable of the subframe interchange.

The motivation to do so would have been to accommodate a multi-stage digital cross connect switch and to take advantage of the time slot interchangers and the space switch capable of the subframe interchange, as suggested by Buttle et al in Col. 5, lines 30- 52.

Regarding claims 11-12, 24-25, as discussed above, Field et al. further teaches that this synchronous switch system and method is applied to SONET STS-M frames

and the interchange random access memory are supported (See Fig. 2, Col. 5, lines 43-65).

Allowable Subject Matter

5. Claim 29 is allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Chang whose telephone number is (571) 272-3129. The examiner can normally be reached on Monday - Friday from 8 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wing Chan can be reached on (571) 272-7493. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

rkc

Richard Chang
Patent Examiner
Art Unit 2616

WING CHAN
SUPERVISORY PATENT EXAMINER